In the Claims:

1. (previously presented): A method of reducing interference in a circuit having a PLL, wherein the circuit is formed on an integrated circuit, the method comprising the steps of:

providing a divider circuit at the input of the PLL for dividing the frequency of an input signal by a desired amount; and

wherein the divider circuit is provided by placing first and second fixed-value dividers connected in series at the input of the PLL.

Claim 2 (canceled)

3. (currently amended): The method of claim 1 ~~claim 2~~, wherein the one of the dividers divides the input frequency by thirteen and the other divider divides the input frequency by five.

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4. (previously presented): The method of claim 1, wherein:

the PLL is powered by a first voltage;

the divider circuit is powered by a second voltage; and

the second voltage is less than the first voltage.

5. (withdrawn): A method of reducing interference present in a circuit comprising the step of:

reducing mutual inductance between digital circuitry in a first portion of the circuit and circuitry in a second portion of the circuit by placing a filter between the digital circuitry and a voltage source external to the circuit in order to reduce the area of a high frequency current loop.

6. (withdrawn): The method of claim 5, wherein the circuit is formed on an integrated circuit, and wherein the first portion of the circuit includes PLL digital circuitry and the second portion includes a VCO.

7. (withdrawn): The method of claim 5, wherein the filter is a low pass filter.

8. (withdrawn): The method of claim 5, wherein the filter creates a secondary current loop for confining current at a desired frequency in the secondary current loop.

9. (withdrawn): The method of claim 8, wherein the filter creates a third current loop for confining current at a desired frequency in the third current loop.

10. (withdrawn): The method of claim 5, wherein the filter is provided by placing a capacitor across first and second nodes in the digital circuitry and placing a resistor between the first node and the voltage source.

11. (withdrawn): The method of claim 10, wherein the filter is further provided by placing a second capacitor between the second node and the resistor and placing a second resistor between the first resistor and the voltage source.

Claims 12-29. (canceled)

30. (withdrawn): A method of reducing interference present in a circuit, the circuit having a plurality of similar circuit elements, the method comprising the step of:

forming at least some of the similar circuit elements on the circuit such that adjacent circuit elements are mirror images of one another.

31. (withdrawn): The method of claim 30, wherein the circuit is formed on an integrated circuit having PLL and VCO circuitry for a wireless communications system.

32. (withdrawn): The method of claim 30, wherein the circuit elements are flip flops.

33. (withdrawn): The method of claim 32, wherein the flip flops form counters for the PLL.

Claims 34-40 (canceled)

41. (withdrawn): A method of reducing interference present in a circuit formed on an integrated circuit having PLL and VCO circuitry, the method comprising the step of:

creating replica circuitry of first circuitry in the circuit which has an impedance that changes state during operation of the circuit, wherein the replica circuitry operates in an opposite state relative to the first circuitry.

42. (withdrawn): The method of claim 41, wherein the replica circuitry has no function in the circuit other than reducing interference.

43. (withdrawn): The method of claim 41, wherein the first circuitry is comprised of a first inverter having a high state and a low state, wherein the replica circuitry is comprised of a second inverter having a high state and a low state, and wherein the second inverter is controlled to be in the opposite state of the first inverter.

44. (withdrawn): The method of claim 41, wherein the replica circuitry is comprised of circuitry similar to the first circuitry, the method further comprising the step of connecting an inverter between an input of the first circuitry and an input of the replica circuitry.

Claims 45-51 (canceled)

52. (previously presented): A method of integrating VCO and PLL circuitry for a wireless communication system onto a single integrated circuit comprising the steps of:

forming an integrated circuit having both PLL circuitry and VCO circuitry integrated on the integrated circuit; and

applying one or more techniques to reduce interference present near the frequency of an output of the VCO.

53. (previously presented): The method of claim 52, wherein the one or more techniques includes providing fixed divider circuitry for the PLL.

54. (previously presented): The method of claim 53, wherein the divider circuitry further comprises first and second series connected fixed dividers.

55. (withdrawn): The method of claim 52, wherein the one or more techniques includes reducing the mutual inductance between digital circuitry in the PLL and the VCO circuitry by placing a filter between digital circuitry in the PLL and a voltage source external to the integrated circuit in order to reduce the area of a high frequency current loop.

56. (withdrawn): The method of claim 52, wherein the one of the one or more techniques includes:

identifying a conductive trace on the integrated circuit carrying high frequency digital current; and

placing a conductive strip in the proximity of the identified conductive trace to help contain the high frequency digital current flowing through the conductive trace.

57. (withdrawn): The method of claim 52, wherein the integrated circuit includes a plurality of similar circuit elements, and wherein one of the one or more techniques includes forming at least some of the similar circuit elements on the integrated circuit such that adjacent circuit elements are mirror images of one another.

58. (withdrawn): The method of claim 52, wherein one of the one or more techniques includes providing a first block of digital circuitry connected to a second block of digital circuitry by a signal line, and inserting buffer circuitry between the first and second blocks of digital circuitry for containing high frequency current within the first block of digital circuitry.

59. (withdrawn): The method of claim 52, wherein one of the one or more techniques includes the steps of:

identifying circuitry in the integrated circuit in which the impedance of the circuitry changes over time during operation of the integrated circuit; and

creating replica circuitry of the identified circuitry which operates in a phase opposite of the identified circuitry.

60. (withdrawn): The method of claim 52, wherein the integrated circuit includes an interface pin, wherein one of the one or more techniques includes the step of:

providing a filter coupled to the interface pin of the integrated circuit to reduce interference caused by signals at the interface pin.

61. (withdrawn): A method of reducing interference present in a circuit formed on an integrated circuit, the method comprising the step of:

providing first circuitry in the circuit, wherein the first circuitry has an impedance that changes state during operation of the circuit; and

creating replica circuitry of the first circuitry, wherein the replica circuitry operates in an opposite state relative to the first circuitry.

62. (withdrawn): The method of claim 61, wherein the replica circuitry has no function in the circuit other than reducing interference.

63. (withdrawn): The method of claim 61, wherein the first circuitry is comprised of a first inverter having a high state and a low state, wherein the replica circuitry is comprised of a second inverter having a high state and a low state, and wherein the second inverter is controlled to be in the opposite state of the first inverter.

64. (withdrawn): The method of claim 61, wherein the replica circuitry is comprised of circuitry similar to the first circuitry, the method further comprising the step of connecting an inverter between an input of the first circuitry and an input of the replica circuitry.

65. (withdrawn): The method of claim 61, wherein the integrated circuit has PLL and VCO circuitry.

66. (new): A method of reducing interference in a circuit formed on an integrated circuit and requiring a divider circuit, the method comprising the steps of:

providing a first fixed-value divider having an input and an output;

providing a second fixed-value divider having an input and an output;

coupling the output of the first fixed-value divider to the input of the second fixed-value divider;

coupling the output of the second fixed-value divider to the circuit;

generating a first output signal by applying an input frequency to the input of the first fixed-value divider to divide the input frequency by a first fixed value; and

generating a second output signal by applying the first output signal to the input of the second fixed-value divider to further divide the input frequency by a second fixed value.

67. (new): The method of claim 66, wherein the product of the first and second fixed values is sixty-five.

68. (new): The method of claim 67, wherein the fixed values are five and thirteen.

69. (new): The method of claim 66, wherein the first and second dividers are non-programmable dividers.

70. (new): The method of claim 66, wherein the first divider is clocked at a first rate, and the second divider is clocked at a second rate.

71. (new): The method of claim 70, wherein the first rate is greater than the second rate.

72. (new): The method of claim 71, wherein the second rate is a function of the first fixed value.

73. (new): The method of claim 66, wherein the first and second dividers are powered by a lower voltage than the remainder of the circuit.

74. (new): The method of claim 66, wherein the circuit includes a PLL.

75. (new): The method of claim 66, wherein the circuit is a frequency synthesizer.

76. (new): The method of claim 66, wherein the circuit is a frequency synthesizer for a wireless communications device.

77. (new): A circuit for reducing interference on an integrated circuit comprising:

circuitry formed on the integrated circuit having an input; and

a divider formed on the integrated circuit and coupled to the input of the circuitry, wherein the divider further comprises:

a first fixed-value divider for receiving an input signal and dividing the input signal by a first amount, and

a second fixed-value divider for receiving the divided signal from the first fixed-value divider and further dividing the input signal by a second amount.

78. (new): The circuit of claim 77, wherein the product of the first and second amounts is sixty-five.

79. (new): The circuit of claim 77, wherein the first amount is five and the second amount is thirteen.

80. (new): The circuit of claim 77, wherein the first and second dividers are non-programmable dividers.

81. (new): The circuit of claim 77, wherein the first and second dividers are clocked at different rates.

82. (new): The circuit of claim 81, wherein the second divider is clocked at a rate that is a function of the first amount.

83. (new): The circuit of claim 77, wherein the circuitry includes a PLL.

84. (new): The circuit of claim 77, wherein the circuitry is a frequency synthesizer.

85. (new): A method of reducing interference in a circuit formed on an integrated circuit comprising the steps of:

identifying a need for a divider in the circuit;

minimizing the number of circuit components required by the divider by using a plurality of fixed-value dividers rather than one or more programmable dividers; and

clocking at least one of the plurality of fixed-value dividers at a slower rate than other fixed-value dividers in the circuit.